

What is Claimed is:

1 1. During the testing of the operation of target
2 processor by a host processing unit, a system for
3 identifying the occurrence of a processor unit reset, the
4 system comprising:

5 timing trace apparatus responsive to signals from the
6 processor unit, the timing trace apparatus generating a
7 timing trace stream;

8 program counter trace apparatus responsive to signals
9 from the processing unit, the program counter trace
10 apparatus generating a program counter trace stream; and

11 synchronization apparatus applying periodic signals to
12 the timing trace apparatus and to the program counter trace
13 apparatus, the periodic signals;

14 wherein the program counter trace apparatus is
15 responsive to a reset signal, the program counter trace
16 apparatus generating reset marker signal group identifying
17 the occurrence of reset signal and relating the reset
18 signal to the timing trace stream and the program
19 execution.

20

21 2. The system as recited in claim 1 wherein the
22 marker signal group includes a program counter address, a
23 timing index and a periodic sync ID.

24

1 3. The system as recited in claim 1 further
2 comprising:

3 data trace apparatus responsive to signals from the
4 processing unit, the data trace apparatus generating a data
5 trace stream, wherein the periodic sync ID signals are
6 applied to the data trace apparatus provide periodic sync
7 markers in the data trace stream; and

8 wherein the host processing unit is responsive to the
9 timing trace stream, the program counter trace stream and
10 the data trace stream, the host processing unit
11 reconstructing the processing activity of the processing
12 unit from the trace streams.

13

14 4. The system as recited in claim 1 wherein the
15 program counter trace apparatus is responsive to the
16 removal of the reset signal, the program counter trace
17 apparatus generating a reset-off marker signal group, the
18 reset-off marker signal group relating the occurrence of
19 the reset signal to the timing trace stream and the program
20 execution.

21

22 5. The method for communicating an occurrence of a
23 reset signal from a target processor unit to a host
24 processing unit, the method comprising:

25 generating a timing trace stream, a program counter
26 trace stream, and data trace stream, and

1 in the program counter trace stream, including a
2 marker signal group indicating an occurrence of reset
3 signal and relating the occurrence to the data trace
4 stream, to the timing trace stream, and to the program
5 execution.

6

7 6. The method as recited in claim 5 further
8 including:

9 in the marker signal group, including a periodic sync
10 ID, a timing index and a program counter address.

11

12 7. The method as recited in claim 5 further
13 comprising, when the reset signal is removed, including in
14 the program counter trace stream a marker signal group
15 indicating the occurrence of the removal of the signal
16 group and relating the marker signal group to the timing
17 trace stream and program execution.

18

19 8. In a processing unit test environment wherein a
20 target processor transmits a plurality of trace streams to
21 a host processing unit, a marker signal group included in a
22 trace signal stream, the marker signal group comprising:

23 indicia of the occurrence of a reset signal;

24 indicia of the relationship of the occurrence of the
25 reset signal to the target processor clock; and

26 indicia of the relationship of the occurrence of the
27 reset signal to the target processor program execution.

1

2 9. In a processing unit test environment wherein a
3 target processor transmits a plurality of trace streams to
4 a host processing unit, a marker signal group included in a
5 trace signal stream, the marker signal group comprising:

6 indicia of the removal of a reset signal;

7 indicia of the relationship of the removal of the
8 reset signal to the target processor clock; and

9 indicia of the relationship of the removal the reset
10 signal to the target processor program execution.

11

12 10. In a target processing unit generating trace test
13 signals for transfer to a host processing unit, program
14 counter trace generation apparatus comprising:

15 a storage unit;

16 a decoder unit responsive to a reset signal for storing
17 a signal group identifying the reset signal in the storage
18 unit in a first location in the storage unit, the decoder
19 unit generating a control signal;

20 a gate unit responsive to the control signal, the gate
21 unit transmitting processor signals applied thereto to the
22 storage unit for storage at defined locations, the signals
23 stored in the storage unit forming a reset sync marker; and

24 a FIFO unit coupled to the storage unit, the FIFO unit
25 receiving the reset sync marker when the reset signal
26 marker is complete, the FIFO unit transferring the reset
27 sync marker to the host processing unit.

1

2 11. The program counter trace apparatus as recited in
3 claim 10 wherein the signals applied to the gate unit
4 include a program counter address, a periodic sync ID, and
5 a timing index.

6

7 12. The program counter trace apparatus as recited in
8 claim 11 wherein when the reset signal is removed, a reset-
9 off sync marker is generated in the storage unit.

10

11 13. The program counter trace apparatus as recited in
12 claim 10 wherein the reset sync marker signal includes a
13 plurality of packets.

14

15 14. The program counter trace apparatus as recited in
16 claim 10 wherein the sync markers in the FIFO unit are
17 transferred from the unit in response to control signals.

18